Remarks/Arguments

There are no amendments to the specification or the drawings hereinabove.

In the claims, Claims 1-25 remain and are pending in the application. Claims 12-20 are allowed. Claims 1, 6 and 21 are rejected and Claims 2-5, 7-11 and 22-25 are objected to. Reconsideration is respectfully requested.

Claim 1 is amended to further recite "an output of the bias generator". Support for the amendment is found at least in Claim 1, as originally filed. No new matter is added. Entry of the amendment is respectfully requested.

The Examiner rejected Claim 1 under 35 U.S.C. 112, first paragraph, contending Claim 1 fails "in a manner similar to that of a 'single means' claim, especially since no details of the device have been recited".

It is respectfully submitted that Amended Claim 1 hereinabove renders moot the Examiner's rejection of Claim 1 under 35 U.S.C. 112, first paragraph. In particular, amended Claim 1 positively recites "an output of the bias generator" as well as a "means for adjusting a set of available magnitudes". Reconsideration and withdrawal of the rejection are respectfully requested.

The Examiner rejected Claims 1, 6 and 21 under 35 U.S.C. 102(e) as being anticipated by Marr, U.S. Patent No. 6,630,724 (hereinafter 'Marr').

Applicant respectfully traverses the rejection of Claims 1, 6 and 21 in view of Marr on the grounds that the Examiner failed to establish a *prima facie* case of anticipation with respect to Marr. In particular, Applicant submits that Marr fails to disclose, explicitly or implicitly, "each element of the claim under consideration" (*W.L. Gore & Associates v. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983)) and/or fails to disclose the claimed elements "arranged as in the claim" (*Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984)) as required by the Federal Circuit for *prima facie* anticipation under 35 U.S.C. 102.

Regarding base Claim 1, the Examiner contended, "Fig. 4 of Marr discloses a bias generator [440] for testing (Col. 1 lines 28-29) of a static random access memory

SRAM (Fig. 28; Col. 4 lines 65-67) comprising: means [410, 412, 414, 416] for adjusting a set of available magnitudes (Col. 7 lines 29-34) of a bias voltage output signal [422] at an output [*sic*] the bias generator [440] using metal programming (Col. 7 lines 1-6; Col. 8 lines 52-54)".

Marr discloses gate dielectric antifuse circuits and methods for operating the circuits. In particular, Marr discloses, "[a] number of antifuse support circuits and methods for operating them" (Marr, Abstract, lines 1-2). In particular, at Col. 7, lines 29-34, relied upon by the Examiner, Marr discloses, "antifuses 100, 140, 150, 200, and 250 may be programmed to provide coupling to redundant circuits, to change a configuration of the integrated circuit, to tie a line to a voltage or Vss, or to provide identification for the integrated circuit". Marr further discloses that the disclosed antifuses are programmed "by applying a high voltage across its terminals to rupture the insulator and form an electrical path between the terminals" (Marr, Col. 1, lines 52-54). As such, Marr explicitly discloses antifuses that are 'electrically' programmed after circuit fabrication (Also see, Mar, Col. 5, line 60 through Col. 6, line 1).

However, contrary to that contended by the Examiner, Marr fails to disclose that recited in Applicant's base Claim 1. For example, Marr does not disclose "means for adjusting ... using ***metal programming***", as recited in Applicant's Claim 1 (***emphasis*** added). For example, no portion of the bias generator disclosed by Marr employs ***metal programming***. In fact, Marr never mentions or even implies ***metal programming*** of any device or circuit element or in any context whatsoever, contrary to that contended by the Examiner.

The term 'metal programming' is clearly defined in Applicant's specification as "establishing and/or removing connections in an integrated circuit (IC) by changing a routing pattern of an interconnect layer, preferably a final or 'top' interconnect layer, of the IC during circuit fabrication" (Page 6, lines 10-13, Applicant's specification, as filed). In addition to being clearly defined by Applicant, the definition and subsequent usage of the term 'metal programming' by Applicant are consistent with a conventional understanding of the term in the art.

The antifuses disclosed by Marr are clearly 'programmed' after circuit fabrication using an "elevated voltage" applied to the antifuses by one or more disclosed support circuits. As such, one skilled in the art would not confuse the programming of antifuses with the "metal programming" claimed by Applicant.

Marr further discloses a "bias circuit 440" and use of a "bank 400" of "anitfuses 410, 412, 414, and 416" (or "antifuses 410-416") connected to an output of the bias circuit as "shown in FIG. 4" (Marr, Col. 7, line 59, through Col. 8, line 59). However, contrary to the Examiner's contention, Marr does not disclose a "bias generator for testing of a static random access memory (SRAM)" or "means for adjusting a set of available magnitudes of a bias voltage output signal at the output" of the bias generator, as claimed by Applicant.

With respect to the 'testing of SRAM', at Col. 1, lines 26-29, in part relied upon by the Examiner, Marr discloses, "redundant memory cells may be enabled with fusible elements after fabrication to replace defective memory cells found during a test of fabricated memory devices". Marr make no mention of testing memory cells using a bias generator. Furthermore, Marr fails to indicate that there is any ***specific*** relationship between the SRAM circuit 2800 illustrated in FIG. 28 and the disclosed bias circuit 440 (see Marr, Col. 28, lines 39-64). In fact, Marr is ***silent*** on a use or uses of the disclosed bias circuit 440 illustrated in FIG. 4 and any output signal the bias circuit 440 may or may not produce. Similarly, while at Col. 28, lines 41-44, Marr discloses "[t]he SRAM 2800 may include one or more of the circuits and devices described above with respect to FIGS. 1-25 ...", Marr never discloses how the 'circuits and devices' of FIGS 1-25 are 'included' in or employed with the SRAM 2800. Moreover, Marr never discloses using the bias circuit 440 for testing the SRAM 2800. As such, having failed to disclose a use or an output signal of the bias circuit 440 as well as a specific relationship between the bias circuit 440 and the SRAM 2800, Marr clearly fails to disclose "a bias voltage output signal" and/or the "bias generator for testing a static random access memory", as recited in Applicant's Claim 1.

Marr also fails to disclose "means for adjusting a set of available magnitudes of a bias voltage output signal" as recited in Applicant's Claim 1, contrary to the

Examiner's contention. At Col. 7, lines 29-34, relied upon by the Examiner, Marr discloses several potential uses of antifuses 100, 140, 150, 200 and 250. However, Marr fails to disclose using antifuses to 'adjust a set of available magnitudes of a bias voltage output signal'. For that matter, Marr never mentions 'a set of available magnitudes of a bias voltage output signal' and therefore cannot disclose that antifuses 100, 140, 150, 200, and 25 may be employed as 'means for adjusting' such a set.

Therefore, for at least these reasons, Marr does not and respectfully cannot disclose each element recited in Applicant's Claim 1.

Regarding base Claim 6, the Examiner contended that Marr disclose "a metal-programmable transistor (Fig. 2A [250] ... for antifuses [410-416] on Fig. 4" and relied on Col. 8, lines 52-54. The Examiner further contended that Marr disclose that these antifuses adjust "a set of available magnitudes ... when metal programmed" and relied on Col. 7, lines 29-34 and Col. 9, lines 43-58 of Marr.

Regarding base Claim 21, the Examiner again relied on Col. 7, lines 29-34, and Col. 8, lines 52-54 to contend, "Marr discloses a method of modifying ... comprising [440]: providing a metal-programmable transistor (Fig. 2A [250] of antifuses [410-416] on Fig. 4 ... and metal programming [420] the metal-programmable transistor (Fig. 6) ..."

However, Marr actually fails to disclose each and every element claimed in Applicant's Claims 6 and 21 and/or actually fails to disclose the claimed elements of Claims 6 and 21 arranged as in the claim, as required for establishing *prima facie* anticipation, contrary to the Examiner's contention.

In particular, as discussed hereinabove with respect to the rejection of Claim 1, neither at Col. 7, lines 29-34 nor at Col. 8, lines 52-54 (nor at Col. 9, lines 43-58, and Col. 12, lines 32-42 also), relied upon by the Examiner, does Marr disclose "a metal-programmable transistor that adjusts a set of available magnitudes of a bias voltage output signal at the bias generator output when metal programmed", as recited in Applicant's base Claim 6, contrary to that contended by the Examiner.

Furthermore, Marr at least fails to disclose "providing a metal-programmable transistor in the bias generator" and "metal programming the metal-programmable transistor to connect the transistor to circuitry of the bias generator, such that a corresponding ON state resistance of the metal-programmed transistor is combined with an effective ON state resistance of the circuitry to modify the available magnitudes of the set" as recited in Applicant's base Claim 21, contrary to that contended by the Examiner.

Hence, as discussed hereinabove, the teachings of Marr at least lacks one or more elements recited separately in each of Applicant's base Claims 1, 6 and 21. Applicant respectfully submits that that the Examiner has failed to establish *prima facie* anticipation by Marr of Claims 1, 6 and 21. Having failed to establish *prima facie* anticipation by Marr, Applicant respectfully requests that the Examiner reconsider and withdraw the unsupported rejection thereof under 35 U.S.C. 102(e) for at least the reasons set forth hereinabove.

The Examiner objected to Claims 2-5, 7-11 and 22-25 as being dependent upon rejected base claims. Applicant appreciates the Examiner's acknowledgement of the allowability of Claims 2-5, 7-11 and 22-25 if rewritten in independent form. However, in light of Applicant's remarks hereinabove, Applicant respectfully submits that Claims 2-5, 7-11 and 22-25 are in allowable form, as originally filed. Applicant defers rewriting these claims pending the Examiner's consideration of the remarks presented hereinabove for the respective base claims.

Further, Applicant appreciates the Examiner's allowance of Claims 12-20, as filed.

In summary, Claims 1-25 were pending. Claims 12-20 were allowed, Claims 1, 6 and 21 were rejected, and Claims 2-5, 7-11 and 22-25 were objected to. Applicant has amended Claim 1 herein. It is respectfully requested that Claims 1-11 and 21-25 be allowed along with allowed Claims 12-20, and that the application be passed to issue at an early date.

Should the Examiner's action be other than allowance, the undersigned respectfully requests a telephone call from the Examiner to discuss further consideration that would expedite the prosecution of the application. Furthermore,

should the Examiner have any questions regarding the above, please contact the undersigned, J. Michael Johnson, Agent for Applicant, at telephone number (775) 849-3085.

Respectfully submitted,
BLAINE STACKHOUSE ET AL.

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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date shown below.

 3/28/05

J. Michael Johnson Date

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